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Gp/2152
04-3-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Laurence B. Boucher et al.		Ser. No:	09/692,561
Filing Date:	October 18, 2000	Examiner:	Unknown
Atty. Docket No:	ALA-002A	GAU:	2152

For: INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD FOR ACCELERATED PROTOCOL PROCESSING

January 7, 2002

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Assistant Commissioner for Patents
Washington, D.C. 20231

Supplemental Information Disclosure Statement per 37 C.F.R. §1.98

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, applicants bring the following documents to the Examiner's attention. Copies of these documents were enclosed with Information Disclosure Statements filed in parent U.S. Patent Application Ser. No. 09/067,544, or in an International Search Report dated April 1, 1999 for related International Patent Application No. PCT/US98/24943. A form PTO-1449 listing these documents is enclosed herewith.

Citation of these documents shall not be construed as an admission that the documents are prior art with respect to the instant invention, a representation that a search has been made, or an admission that the information cited herein is, or is considered to be, material to patentabilty as defined in 37 C.F.R. § 1.56(b).

Patent Documents

1. U.S. Patent No. 4,991,133 to Davis et al. entitled SPECIALIZED COMMUNICATIONS PROCESSOR FOR LAYERED PROTOCOLS.
2. U.S. Patent No. 5,163,131 to Row et al. entitled PARALLEL I/O NETWORK FILE SERVER ARCHITECTURE.
3. U.S. Patent No. 5,212,778 to Dally et al. entitled MESSAGE DRIVEN PROCESSOR IN A CONCURRENT COMPUTER.

4. U.S. Patent No. 5,289,580 to Latif et al. entitled PROGRAMMABLE MULTIPLE I/O INTERFACE CONTROLLER.
5. U.S. Patent No. 5,303,344 to Yokoyama et al. entitled PROTOCOL PROCESSING APPARATUS FOR USE IN INTERFACING NETWORK CONNECTED COMPUTER SYSTEMS UTILIZING SEPARATE PATHS FOR CONTROL INFORMATION AND DATA TRANSFER.
6. U.S. Patent No. 5,412,782 to Hausman et al. entitled PROGRAMMED I/O ETHERNET ADAPTER WITH EARLY INTERRUPTS FOR ACCELERATING DATA TRANSFER.
7. U.S. Patent No. 5,485,579 to Hitz et al. entitled MULTPLE FACILITY OPERATING SYSTEM ARCHITECTURE.
8. U.S. Patent No. 5,506,966 to Ban entitled SYSTEM FOR MESSAGE TRAFFIC CONTROL UTILIZING PRIORITIZED MESSAGE CHAINING FOR QUEUEING CONTROL ENSURING TRANSMISSION/RECEPTION OF HIGH PRIORITY MESSAGES.
9. U.S. Patent No. 5,511,169 to Suda entitled DATA TRANSMISSION APPARATUS AND A COMMUNICATION PATH MANAGEMENT METHOD THEREFOR.
10. U.S. Patent No. 5,548,730 to Young et al. entitled INTELLIGENT BUS BRIDGE FOR INPUT/OUTPUT SUBSYSTEMS IN A COMPUTER SYSTEM.
11. U.S. Patent No. 5,566,170 to Bakke et al. entitled METHOD AND APPARATUS FOR ACCELERATED PACKET FORWARDING.
12. U.S. Patent No. 5,588,121 to Reddin et al. entitled PARALLEL COMPUTER HAVING MAC-RELAY LAYER SNOOPED TRANSPORT HEADER TO DETERMINE IF A MESSAGE SHOULD BE ROUTED DIRECTLY TO TRANSPORT LAYER DEPENDING UPON ITS DESTINATION.
13. U.S. Patent No. 5,590,328 to Seno et al. entitled PROTOCOL PARALLEL PROCESSING APPARATUS HAVING A PLURALITY OF CPUs ALLOCATED TO PROCESS HIERARCHICAL PROTOCOLS.
14. U.S. Patent No. 5,592,622 to Isfeld et al. entitled NETWORK INTERMEDIATE SYSTEM WITH MESSAGE PASSING ARCHTECTURE.

15. U.S. Patent No. 5,634,099 to Andrews et al. DIRECT MEMORY ACCESS UNIT FOR TRANSFERRING DATA BETWEEN PROCESSOR MEMORIES IN MULTIPROCESSING SYSTEMS.

16. U.S. Patent No. 5,642,482 to Pardillos entitled SYSTEM FOR NETWORK TRANSMISSION USING A COMMUNICATION COPROCESSOR COMPRISING A MICROPROCESSOR TO IMPLEMENT PROTOCOL LAYER AND A MICROPROCESSOR TO MANAGE DMA.

17. U.S. Patent No. 5,671,355 to Collins entitled RECONFIGURABLE NETWORK INTERFACE APPARATUS AND METHOD.

28. U.S. Patent No. 5,692,130 to Shobu et al. entitled METHOD FOR SELECTIVELY USING ONE OR TWO COMMUNICATION CHANNEL BY A TRANSMITTING DATA TERMINAL BASED ON DATA TYPE AND CHANNEL AVAILABILITY.

19. U.S. Patent No. 5,699,317 to Sartore et al. entitled ENHANCED DRAM WITH ALL READS FROM ON-CHIP CACHE AND ALL WRITERS TO MEMORY ARRAY.

20. U.S. Patent No. 5,701,434 to Nakagawa entitled INTERLEAVE MEMORY CONTROLLER WITH A COMMON ACCESS QUEUE.

21. U.S. Patent No. 5,749,095 to Hagersten entitled MULTIPROCESSING SYSTEM CONFIGURED TO PERFORM EFFICIENT WRITE OPERATIONS.

22. U.S. Patent No. 5,752,078 to Delp et al. entitled SYSTEM FOR MINIMIZING LATENCY DATA RECEPTION AND HANDLING DATA PACKET.

23. U.S. Patent No. 5,758,084 to Silverstein et al. entitled APPARATUS FOR PARALLEL CLIENT/SERVER COMMUNICATION HAVING DATA STRUCTURES WHICH STORED VALUES INDICATIVE OF A CONNECTION STATE AND ADVANCING THE CONNECTION STATE OF ESTABLISHED CONNECTIONS.

24. U.S. Patent No. 5,758,089 to Gentry et al. entitled METHOD AND APPARATUS FOR BURST TRANSFERRING ATM PACKET HEADER AND DATA TO A HOST COMPUTER SYSTEM.

25. U.S. Patent No. 5,758,186 to Hamilton et al. entitled METHOD AND APPARATUS FOR GENERICALLY HANDLING DIVERSE PROTOCOL METHOD CALLS IN A CLIENT/SERVER COMPUTER SYSTEM.
26. U.S. Patent No. 5,758,194 to Kuzma entitled COMMUNICATION APPARATUS FOR HANDLING NETWORKS WITH DIFFERENT TRANSMISSION PROTOCOLS BY STRIPPING OR ADDING DATA TO THE DATA STREAM IN THE APPLICATION LAYER.
27. U.S. Patent No. 5,790,804 to Osborne entitled COMPUTER NETWORK INTERFACE AND NETWORK PROTOCOL WITH DIRECT DEPOSIT MESSAGING.
28. U.S. Patent No. 5,812,775 to Van Seeters et al. entitled METHOD AND APPARATUS FOR INTERNETWORKING BUFFER MANAGEMENT.
29. U.S. Patent No.5,878,225 to Bilansky et al. entitled DUAL COMMUNICATION SERVICES INTERFACE FOR DISTRIBUTED TRANSACTION PROCESSING.
30. U.S. Patent No. 5,930,830 to Mendelson et al. entitled SYSTEM AND METHOD FOR CONCATENATING DISCONTIGUOUS MEMORY PAGES.
31. U.S. Patent No. 5,991,299 to Radogna et al. entitled HIGH SPEED HEADER TRANSLATION PROCESSING.
32. U.S. Patent No. 6,061,368 to Hitzelberger entitled CUSTOM CIRCUITRY FOR ADAPTIVE HARDWARE ROUTING ENGINE.
33. U.S. Patent No. 6,034,963 to Minami et al. entitled MULTIPLE NETWORK PROTOCOL ENCODER/DECODER AND DATA PROCESSOR.
34. Provisional U.S. Patent No. 60/053/240 to Jolitz et al.
35. PCT Pat. App. PCT/US97/17257 to Minami et al. entitled MULTIPLE NETWORK PROTOCOL ENCODER/DECODER AND DATA PROCESSOR.
36. PCT Pat. App. PCT/US98/08719 to Poff et al. entitled HARDWARE ACCELERATOR FOR AN OBJECT-ORIENTED PROGRAMMING LANGUAGE.
37. PCT Pat. App. PCT/US98/14729 to Jolitz et al. entitled TPC/IP NETWORK ACCELERATOR SYSTEM AND METHOD.

Other Documents

38. Internet pages entitled Technical White Paper – Xpoint's Disk-to-LAN Acceleration Solution for Windows NT server, printed 6/5/97.

39. Jato Technologies Internet pages entitled Network Accelerator Chip Architecture, twelve-slide presentation, printed 8/19/98.

40. EETIMES article dated August 10, 1998, Issue 1020, entitled Enterprise system uses flexible spec, printed 11/25/98.

41. Internet pages entitled iREADY About Us and iREADY Products, printed 11/25/98.

42. Internet pages entitled Smart Ethernet Network Interface Card which Berend Ozceri is developing, and Internet pages entitled Hardware Assisted Protocol Processing, which Eugene Feinberg is working on, printed 11/25/98.

43. Internet pages of XaQti Corporation entitled GigaPOWER Protocol Processor Product Preview, printed 11/25/98.

44. Internet pages entitled: DART: Fast Application Level Networking via Data-copy Avoidance, by Robert J. Walsh, printed 6/3/99.

45. Internet pages of InterProphet entitled: Frequently Asked Questions, by Lynne Jolitz, printed 6/14/00.

Respectfully submitted,

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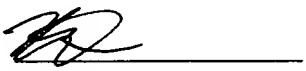
CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on January 7, 2002.

Date: 1-7-02



Mark Lauer

U.S. Department of Commerce, Patent and Trademark Office	Application No.: 09/692,561
	Filing date: October 18, 2000
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Inventors: Laurence B. Boucher et al.
	Group Art Unit: 2152
INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD FOR ACCELERATED PROTOCOL PROCESSING	Examiner name:
	Attorney Docket No. ALA-002A

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U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	AA	4,991,133	5/13/86	Davis et al.	364	900	
	AB	5,163,131	11/10/92	Row et al.	395	200	
	AC	5,212,778	5/18/93	Dally et al.	395	400	
	AD	5,289,580	2/22/94	Latif et al.	395	275	
	AE	5,303,344	4/12/94	Yokoyama et al.	395	200	
	AF	5,412,782	5/2/95	Hausman et al.	395	250	
	AG	5,485,579	1/16/96	Hitz et al.	395	200.12	
	AH	5,506,966	4/9/96	Ban	395	250	
	AI	5,511,169	4/23/96	Suda	395	280	
	AJ	5,548,730	8/20/96	Young et al.	395	280	
	AK	5,566,170	10/15/96	Bakke et al.	370	60	

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Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL	WO 98/19412	5/7/98	PCT/US97/17257				
	AM	WO/9850852	11/12/98	PCT/US98/08719				
	AN	WO 99/04343	1/28/99	PCT/US98/14729				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AO	Internet pages entitled: Technical White Paper - Xpoint's Disk to LAN Acceleration Solution for Windows NT Server, printed 6/5/97.
	AP	Jato Technologies Internet pages entitled: Network Accelerator Chip Architecture, twelve-slide presentation, printed 8/19/98.
	AQ	EETIMES article entitled: Enterprise System Uses Flexible Spec, dated August 10, 1998, printed 11/25/98.
	AR	Internet pages entitled iReady About Us and iReady Products, printed 11/25/98.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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COPY OF PAPERS ORIGINALLY FILED

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	AA	5,588,121	12/24/96	Reddin et al.	395	200.15	
	AB	5,590,328	12/31/96	Seno et al.	395	675	
	AC	5,592,622	1/7/97	Isfeld et al.	395	200.02	
	AD	5,634,099	5/27/97	Andrews et al.	395	200.07	
	AE	5,642,482	6/24/97	Pardillos	395	200.2	
	AF	5,671,355	9/23/97	Collins	395	200.2	
	AG	5,692,130	11/25/97	Shobu et al.	395	200.12	
	AH	5,699,317	12/16/97	Sartore et al.	395	230.06	
	AI	5,701,434	12/23/97	Nakagawa	395	484	
	AJ	5,749,095	5/5/98	Hagersten	711	141	
	AK	5,752,078	5/12/98	Delp et al.	395	82	

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Foreign Patent Documents

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	AL							
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	AN							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AO	Internet pages entitled: Smart Ethernet Network Interface Cards which Berend Ozceri is developing, and Internet pages entitled: Hardware Assisted Protocol Processing, which Eugene Feinberg is working on, printed 11/25/98.
	AP	Internet pages of Xaqti corporation entitled: GigaPower Protocol Processor Product review, printed 11/25/09
	AQ	Internet pages entitled: DART: Fast Application Level Networking via Data-copy Avoidance, by Robert J. Walsh, printed 6/3/99.
	AR	Internet pages of InterProphet entitled: Frequently Asked Questions, by Lynne Jolitz, printed 6/14/00.

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	AA	5,758,084	5/26/98	Silverstein et al.	395	200.58	
	AB	5,758,089	5/26/98	Gentry et al.	395	200.64	
	AC	5,758,186	5/26/98	Hamilton et al.	395	831	
	AD	5,758,194	5/26/98	Kuzma	395	886	
	AE	5,790,804	8/4/98	Osborne	395	200.75	
	AF	5,812,775	9/22/98	Van Seeters et al.	395	200.43	
	AG	5,878,225	3/2/99	Bilansky et al.	395	200.57	
	AH	5,930,830	7/27/99	Mendelson et al.	711	171	
	AI	5,991,299	11/23/99	Radogna et al.	370	392	
	AJ	6,061,368	5/9/00	Hitzelberger	370	537	
	AK	6,034,963	3/7/00	Minami et al.	370	401	

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OIPE JC1#8 MAR 07 2002 PATENT & TRADEMARK OFFICE

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	AA	60/053,240		Jolitz et al.			7/18/97
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